ABSTRACT OF THE DISCLOSURE

[0025] A chip stack comprising at least two carrier layers, each of which includes a first conductive pattern disposed thereon. The chip stack further comprises at least one thermal ring having a second conductive pattern disposed thereon. The thermal ring is formed to include at least two flow channels. The thermal ring is disposed between the carrier layers, with the second conductive pattern being electrically connected to the first conductive pattern of each of the carrier layers. Also included in the chip stack are at least two integrated circuit chips which are electrically connected to respective ones of the first conductive patterns. One of the integrated circuit chips is circumvented by the thermal ring and disposed between the carrier layers. The flow channels within the thermal ring facilitate the circulation of cooling air over the integrated circuit chip disposed between the carrier layers.